operation performed when fuse circuits FC0 and FC3 are cut off in the refresh cycle control circuit shown in Fig. 11; and

Fig. 13 is a functional block diagram showing the configurations of a refresh cycle control circuit, a row decoder, and a virtual word line decoder and word line driver in a DRAM according to a fourth embodiment of the present invention.

4. Claims

1. A dynamic semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells, the memory cell array being divided into a plurality of blocks;

a block decoder for decoding row address signals and producing block selection signals;

a refresh cycle control circuit for dividing the block selection signals by preset frequency dividing ratios to set refresh cycles for the blocks; and

a row decoder for selecting the blocks in response to the block selection signals.

2. The dynamic semiconductor memory device according to Claim 1, wherein the refresh cycle control circuit comprises:

a fuse circuit for setting the frequency dividing ratios; and

a frequency divider for dividing the block selection signals by frequency dividing ratios set in the fuse circuit.

3. The dynamic semiconductor memory device according to Claim 2, wherein the fuse circuit is formed on the row decoder.

4. A dynamic semiconductor memory device comprising:

a memory cell array including a plurality of memory cells, the memory cell array being divided into a plurality of first hierarchical blocks and each of the first hierarchical blocks being further divided into a plurality of second hierarchical blocks; and

a refresh cycle setting means for setting a first refresh cycle for the first hierarchical blocks and a second refresh cycle for the second hierarchical blocks.

5. The dynamic semiconductor memory device according to Claim 4, further comprising:
a row decoder for selecting one of the first hierarchical blocks in response to a first block selection signal and for selecting one of the second hierarchical blocks in the selected first hierarchical block in response to a second block selection signal,

wherein the refresh cycle setting means comprises:

a first frequency divider for dividing the first block selection signal by a predetermined first frequency dividing ratio; and

a second frequency divider for dividing the second block selection signal by a predetermined second frequency dividing ratio.

6. The dynamic semiconductor memory device according to Claim 5, wherein
the refresh cycle setting means further comprises:
a first fuse circuit for setting the first frequency dividing ratio; and
a second fuse circuit for setting the second frequency dividing ratio.

7. The dynamic semiconductor memory device according to Claim 6, wherein the first and second fuse circuits are formed on the row decoder.

8. The dynamic semiconductor memory device according to Claim 4, further comprising:

a row decoder for selecting one of the first

hierarchical blocks in response to a first block selection signal and for selecting one of the second hierarchical blocks in the selected first hierarchical block in response to a second block selection signal,

wherein the refresh cycle setting means comprises:

a frequency divider for dividing the second block selection signal by a predetermined first or second frequency dividing ratio.

9. The dynamic semiconductor memory device according to Claim 8, wherein

the refresh cycle setting means further comprises:

a fuse circuit for setting the first or second frequency dividing ratio.

10. The dynamic semiconductor memory device according to Claim 9, wherein

the fuse circuit is formed on the row decoder.